2 T855 Circuit Operation

This section provides a basic description of the circuit operation of the T855 receiver.

Refer to Section 6 where the parts lists, grid reference index and diagrams will provide detailed information on identifying and locating components and test points on the main PCB. The parts lists and diagrams for the memory and VCO PCBs are in Part E.

The following topics are covered in this section.

2.1 Introduction

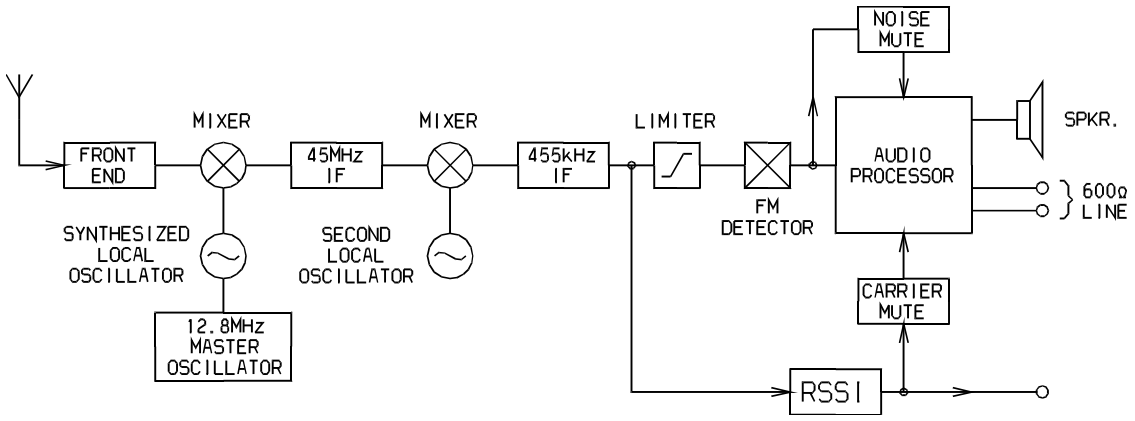

Figure 2.1 T855 High Level Block Diagram

The T855 receiver consists of a number of distinct stages:

- front end
- mixer
- synthesised local oscillator
- IF
- audio processor
- mute (squelch)
- regulator circuits
- received signal strength indicator (RSSI).

These stages are clearly identifiable in Figure 2.1. Refer to the circuit diagrams in Section 6 for further detail.

2.2 Receiver Front End

(Refer to the receiver and audio processor circuit diagrams in Section 6.)

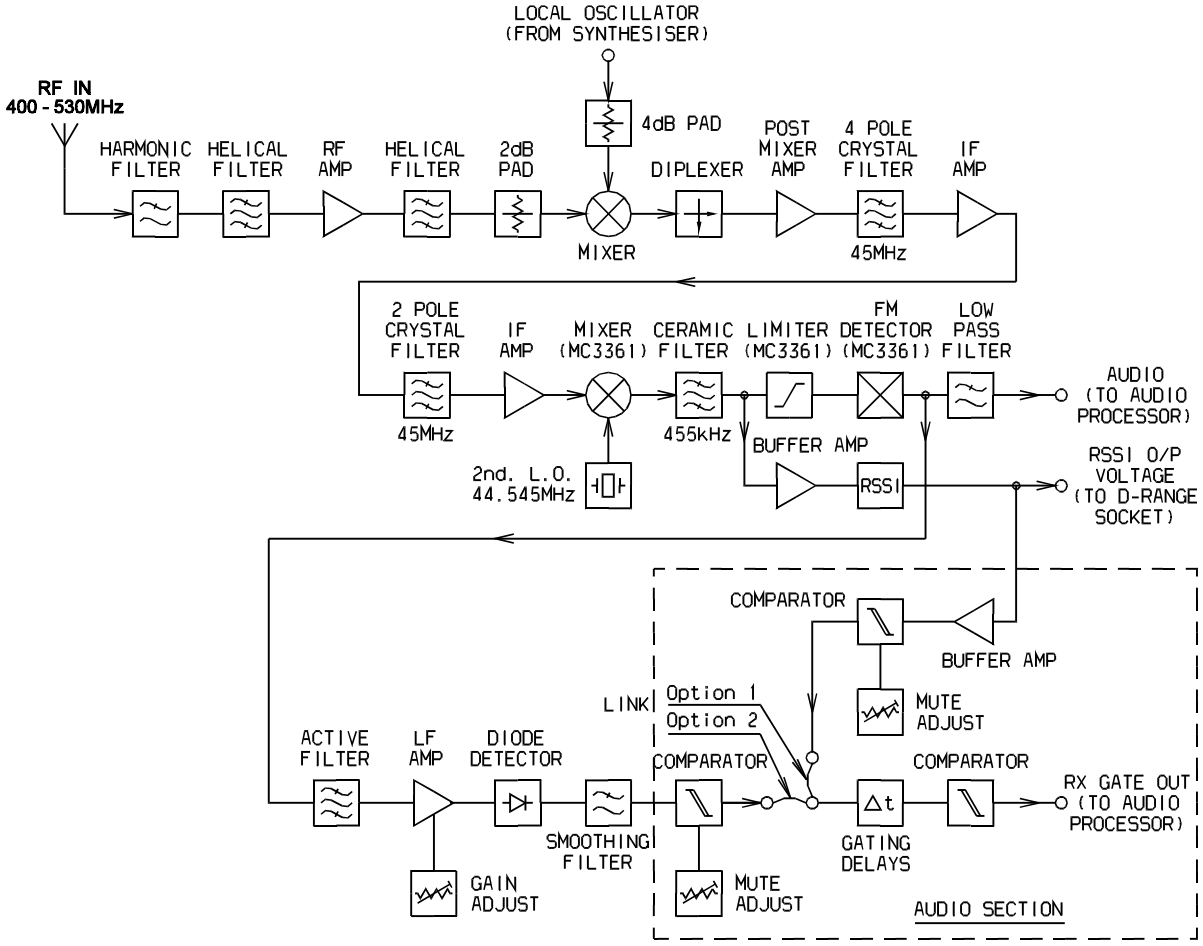

Figure 2.2 T855 Front End, IF and Mute Block Diagram

The incoming signal from the N-type antenna socket is fed through a 9-pole, low pass filter with a cut frequency of approximately 600MHz. This low loss filter (typically less than 0.5dB over 400-530MHz) provides excellent immunity to interference from high frequency signals.

The signal is then further filtered, using a high performance helical resonator doublet (FL300) which provides exceptional image rejection, before being amplified by approximately 8dB (Q303). The signal is then passed through a further helical filter doublet (FL301) before being presented to the mixer via a 2dB attenuator pad.

Each sub-block within the front end has been designed with 50 ohm terminations for ease of testing and fault finding. The overall gain from the antenna socket to the mixer input is approximately 2dB.

2.3 Mixer

(Refer to the receiver circuit diagram in Section 6 and Figure 2.2.)

IC301 is a high level mixer requiring a local oscillator (LO) drive level of +17dBm (nominal). The voltage controlled oscillator (VCO) generates a level of +20dBm (typical) and this is fed to the mixer via a 4dB attenuator pad. A diplexer terminates the IF port of the mixer in a good 50 ohms, thus preventing unnecessary intermodulation distortion.

2.4 IF Circuitry

(Refer to the receiver circuit diagram in Section 6 and Figure 2.2.)

Losses in the mixer are made up for in a tuned, common gate, post mixer amplifier (Q305). Several stages of amplification and filtering are employed in the IF circuitry. The first crystal filter is a 4-pole device (&XF300) which is matched into 50 ohms on both its input and output ports. This stage is followed by a common base amplifier (Q302) whose output is matched into a 2-pole crystal filter (&XF301). The signal is then amplified using a high gain MOSFET amplifier (Q304) before being mixed down to 455kHz with the second local oscillator (44.545MHz).

The 455kHz signal is filtered using a 6-pole ceramic filter (&XF302) before being limited and detected. Q306 provides a buffered 455kHz output for use with the optional RF level detector (RSSI).

The second IF mixer, limiter and detector is in a 16-pin IC (IC300). Quadrature detection is employed, using L316, and the recovered audio on pin 9 of IC300 is typically 1V p-p for 60% system deviation.

2.5 Noise Mute (Squelch)

(Refer to the receiver circuit diagram in Section 6 and Figure 2.2.)

The noise mute operates on the detected noise outside the audio bandwidth. The operational amplifier in IC300 is used as an active band pass filter centred on 70kHz to filter out audio components. The noise spectrum is then further amplified in a variable gain, two-stage amplifier (Q300 & Q301) with additional filtering. The noise is then rectified (D300) and filtered to produce a DC voltage proportional to the noise amplitude. The lowest average DC voltage corresponds to a high RF signal strength and the highest DC voltage corresponds to no signal at the RF input.

The rectified noise voltage is compared with a threshold voltage set up on RV100, the front panel mute potentiometer. Hysteresis is introduced by the feedback resistor (R106) to prevent the received message from being chopped when the average noise voltage is close to the threshold. R111 and R110 determine the mute opening and closing times. The mute control signal at pin 7 of IC100 is used to disable the speaker and line audio outputs. The speaker output can be separately enabled for test purposes by operating the front panel mute disable switch, SW100.

The mute control line is available on pad 101 (Rx gate out) for control of external circuitry. A high (9V) on pad 101 indicates that the audio is disabled and a low (0V) indicates that a signal above the mute threshold level is being received.

The audio can also be disabled using the "Rx-disable" inputs, pads 100 or 113, having connected the "Rx-disable" link between pins 1 & 2 of PL100. An adjustable time delay (RV101) is provided on these lines. In order to disable the audio, either pad must be pulled to 0V.

The red front panel LED (D102) indicates the status of the mute circuit. When a signal above the mute threshold is received, the LED is illuminated. An undedicated relay is provided (RL100) for transmitter keying or other functions and this can be operated from the mute line by linking PL102.

2.6 Carrier Mute

(Refer to the receiver circuit diagram in Section 6 and Figure 2.2.)

A high level carrier mute facility is also available when the RSSI option PCB is fitted. The RSSI (refer to Section 2.10) provides a DC voltage proportional to the signal strength. This voltage is compared with a preset level, set up on RV104, and may be linked into the mute timing circuit using PL104. PL104 selects either the noise mute or the carrier mute. From this point both mute circuits operate in the same manner, using common circuitry.

2.7 Audio Processor

(Refer to the audio processor circuit diagram in Section 6.)

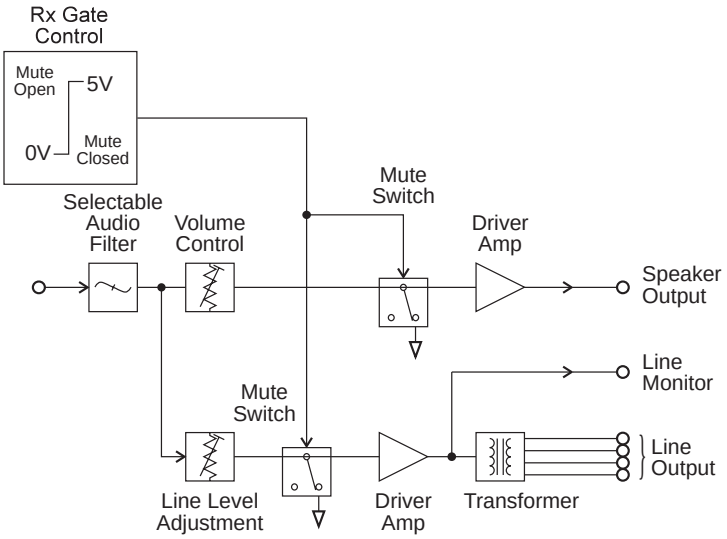

Figure 2.3 T855 Audio Processor Block Diagram

The recovered audio on pin 9 of IC300 is processed in a third order elliptic active filter to give the required response. Linking (PL101 & PL103) is available to give either a flat or de-emphasised audio response, with de-emphasis giving a 6dB / octave roll off. The output of IC101 is split to provide separate paths for the speaker and line outputs.

The speaker volume is set using the front panel volume knob (RV103) and the line level is set using the recessed potentiometer (RV102). The signals are passed to audio drive amplifiers IC102 and IC103. Under muted conditions the inputs of these amplifiers are shunted to ground via transistors Q105 and Q106 respectively.

The audio output of IC102 has a DC component which is removed by C122, and this then drives a speaker directly. The output of IC103 is fed into a line transformer to provide a balanced 2-wire or 4-wire, 600 ohm output.

2.8 Power Supply And Regulator

(Refer to the regulator circuit diagram in Section 6.)

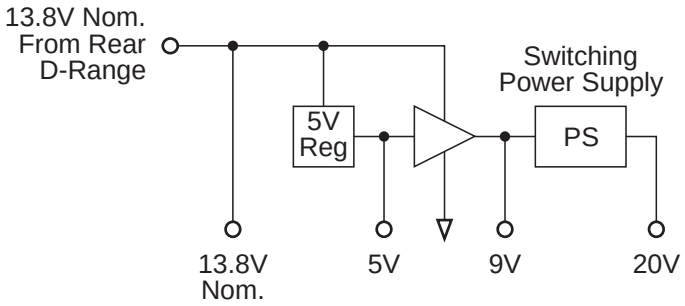

Figure 2.4 T855 Power Supply And Regulator Block Diagram

The T855 is designed to operate off a 10.8-16V DC supply (13.8V nominal). A 5.3V regulator (IC202) runs directly off the 13.8V rail, driving much of the synthesiser circuitry. This is used as the reference for a DC amplifier (IC201, Q200 & Q201) which provides a medium current capability 9V supply. A switching power supply, based on Q202 and Q203, runs off the 9V supply and provides a low current capability +20V supply. This is used to drive the synthesiser loop filter (IC4), giving a VCO control voltage of up to 20V. The 13.8V supply drives both output audio amplifiers without additional regulation.

2.9 Synthesised Local Oscillator

(Refer to the synthesiser circuit diagram in Section 6 and the VCO circuit diagram in Part E.)

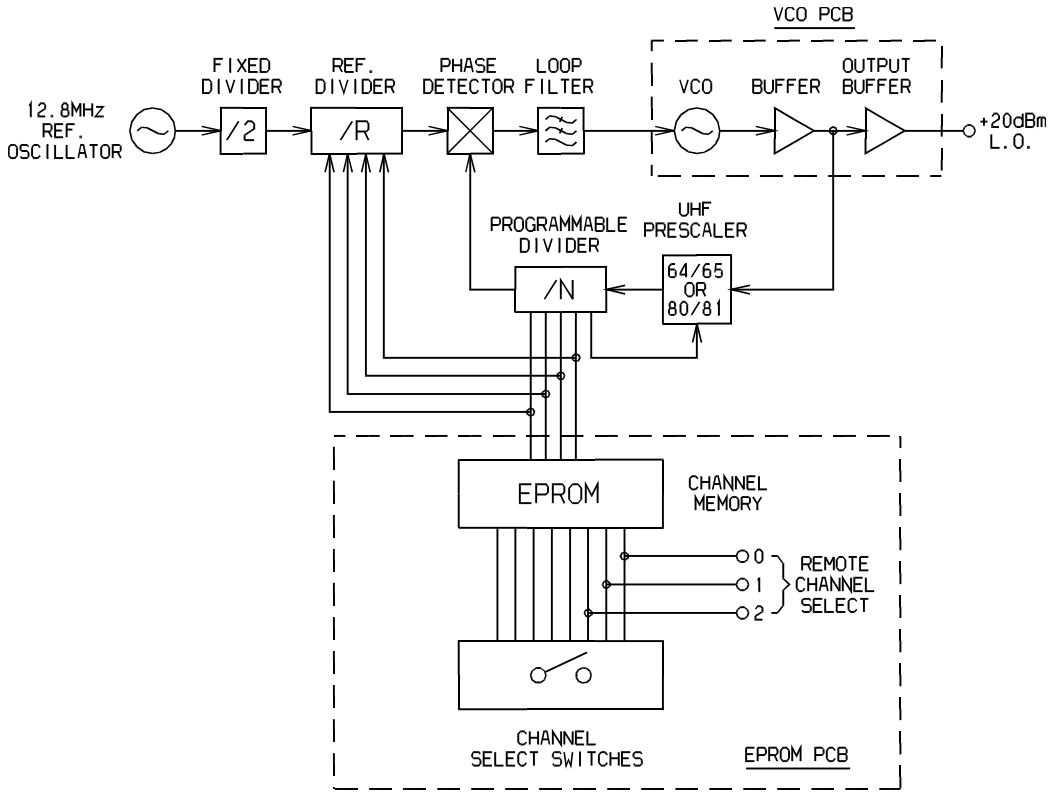

Figure 2.5 T855 Synthesiser Block Diagram

The synthesiser employs a phase-locked loop (PLL) to lock a VCO to a given reference frequency.

A reference oscillator at 12.8MHz (=IC2) is buffered, divided by two and then divided down to 12.5kHz or 6.25kHz within the synthesiser IC (IC3). A buffered output of the VCO is fed to a programmable divider, comprising a UHF prescaler (&IC1) and a divider internal to IC3. These two signals are applied to the phase detectors in IC3. A digital phase detector PDB (IC3 pin 2) provides rapid coarse tuning of the VCO until the phase error is within the range of the high gain sample and hold detector PDA (IC3 pin 1). The phase detector outputs are passed through an active loop filter (IC4a) which produces a DC voltage between 0 and 20V to tune the VCO. This VCO control line is further filtered to attenuate noise and spurs. As the control line voltage increases, the VCO frequency also increases.

The division ratio of the programmable divider is stored within EPROM memory (IC1). Up to 128 frequencies can be stored within the memory and are addressable using the internal DIP switches. Three of the address lines are also available for external frequency control via an extra D-range connector at the rear of the chassis. A change of state of any of these three lines (CH SEL 0-2) commences a programming cycle during which the frequency data in the EPROM is down-loaded to a divider within IC3. 32 bits of data are loaded in eight 4-bit words.

The VCO transistor (Q1) operates in common source and uses a transmission line resonator (TL1). The transmission line is used in a two port configuration with varicaps

positioned at one end. The VCO control voltage from the loop filter (IC4a) is applied to the varicaps (D1 & D2) to facilitate tuning. The VCO output is coupled into a cascode amplifier stage (Q2, Q3) which gives a +10dBm (nominal) output. This output is used to drive the divider buffer for the UHF prescaler which is either a divide by 64/65 for 25kHz channel increments or divide by 80/81 for 12.5kHz channel increments. Further amplification in Q5 brings the output drive level to +20dBm to drive the mixer.

The VCO frequency spans from either 355-395MHz, 395-435MHz or 435-475MHz according to version. The VCO is tuned to 45MHz below the desired receive frequency to produce a 45MHz IF signal on the output of the mixer.

2.10 Received Signal Strength Indicator (RSSI)

(Refer to the receiver circuit diagram in Section 6.)

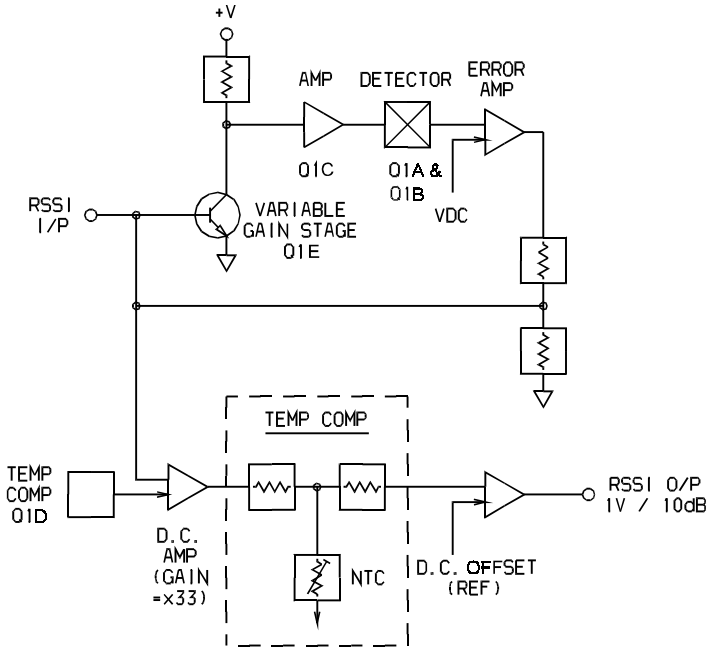

Figure 2.6 T855 RSSI Block Diagram

The RSSI option PCB plugs directly into the main PCB (support circuitry being fitted as standard). It is fitted to the T855 whenever receiver signal strength monitoring is required, e.g. trunking or voting. Its function is to provide a DC voltage proportional to the signal level at the receiver input.

The variable gain stage (Q1A) is a common emitter amplifier with its emitter grounded and the AGC control loop voltage applied to its base. Since the AGC loop will maintain a constant signal level at the collector, the gain of Q1 must be proportional to the incoming 455kHz signal level. The gain of Q1 is linearly proportional to its collector current which itself is exponentially related to the base-emitter voltage. Thus there is a logarithmic relationship between the base-emitter voltage and the gain. The circuit therefore produces a feedback voltage, and an output voltage, logarithmically related to the RF input signal.

The AGC loop is followed by a DC amplifier which provides level shifting, temperature

compensation and gain to give a nominal 1V/10dB at the RSSI output. RV301 on the main PCB is used to set the RSSI voltage to a fixed value at a given RF input signal strength.

2.11 High Sensitivity Preamplifier

(Refer to the preamplifier circuit diagram in Section 6. Refer to fitting instructions in Section A7)

The high sensitivity preamplifier option PCB fits onto the main PCB. It is a single stage broad band low noise preamplifier offering a 3dB improvement in sensitivity with a minimum degradation of other parameters. All performance figures still meet the ETS 300 086:1991 specifications for base stations.

The amplifier fits inside the receiver between the aerial input filter and the first helical filter. Power is derived from the regulated +9v supply.

A table of typical results is given below.

Amplifier Performance	Unmodified T855	T855 With Preamp Fitted	T855 With Modified Preamp Fitted (See Note)
De-emphasised Sensitivity	-117dBm @ 12dB Sinad	-119dBm @ 12dB Sinad	-121dBm @ 12dB Sinad
Flat Audio Sensitivity (CCITT Weighted)	-107 dBm @ 20dB Sinad	-110dBm @ 20dB Sinad	-113dBm @ 20dB Sinad
De-emphasised Selectivity	85dB	83dB	81dB
De-emphasised Intermodulation	80dB	76dB	72dB

Note: A modified preamplifier is one which has been fitted with a 100P 0805 chip capacitor across the 10ohm emitter resistor R5 in order to increase the gain.

